REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-20 are currently pending, Claim 1 having been amended. The changes and additions to the claims do not add new matter and are supported by the originally filed specification, for example, on Fig. 1; page 11, lines 23-25; page 12, lines 14-24; and page 15, lines 1-5.

In the outstanding Office Action, Claims 1-5, 10-13, and 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Saito (U.S. Pub. No. 2002/0026553) in view of Texas Instruments ("Product Bulletin: Boundary-Scan Logic," hereafter "TI-BSL"); Claims 6-9 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Kumiko (Japanese Patent No. JP-9064811); and Claims 14-17 were rejected under 35 U.S.C. §103(a) as unpatentable over Saito in view of TI-BSL and Edwards et al. (U.S. Patent No. 6,684,348, hereafter "Edwards").

Applicants thank the Examiner for the courtesy of an interview extended to Applicants' representatives on November 12, 2008. During the interview, the differences between the claims and the applied art were discussed. Further, clarifying claim amendments were also discussed. Arguments and claims similar to those presented during the interview are presented for formal consideration.

With respect to the rejection of Claim 1 under 35 U.S.C. §103(a), Applicants respectfully submit that the amendment to Claim 1 overcomes this ground of rejection. Amended Claim 1 recites, *inter alia*,

> a plurality of function blocks configured to perform signal processing, each function block comprising one or more devices which collectively perform a specified function of the signal processor;

> a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block; and
>
> at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit.

Applicants respectfully submit that the combination of Saito and TI-BSL fails to disclose or suggest at least these features of amended Claim 1.

Saito describes a method for monitoring regions in a processor circuit for bugs. Saito shows in Figs. 4-9, and 11 that functional blocks 21 send and receive signals outside the circuit through selection means 30 or through signal selection circuit 32 (see para. [0032] of Saito). Saito also describes a processor circuit 1 in Fig. 4, and at least one MPU Core 1 in Figs. 5-9, and 11. Saito describes the processor circuit or the MPU Core can send and receive signals to the plurality of functional blocks 21 (see para. [0031] and [0038]). However, Saito never describes that the processor circuit 1 or the MPU Core 1 transmits an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block.

Therefore, Applicants respectfully submit that Saito fails to disclose or suggest "a processing unit configured to transmit an instruction to at least one of the function blocks instructing the at least one of the function blocks to transmit the debug information to the selection multiplex output block," as defined by amended Claim 1.

The Office Action acknowledges that Saito fails to disclose or suggest "at least two of the dedicated paths provided for one of the plurality of function blocks, said paths configured

to transmit input data and output data associated with said one of the plurality of function blocks, as debug information from said one of the plurality of function blocks to the selection multiplex output block," as previously recited in Claim 1 (See Office Action at page 3).

Therefore, Applicants submit that Saito also fails to disclose or suggest "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit," as defined by amended Claim 1.

The Office Action relies on TI-BSL to remedy the deficiencies of Saito with regards to Claim 1. (See Office Action at pages 3-4).

TI-BSL is directed towards boundary-scan logic technology. The figure shown on page 3 of TI-BSL shows a core logic unit that is to be tested within the boundary-scan architecture. Boundary-scan register cells (BSCs) are interconnected between input/output pins and the core logic unit (see page 3 of TI-BSL, sixth full paragraph). During normal operations, input and output signals pass freely through the BSCs from a normal data input to the normal data output. When boundary test mode is entered, the BSCs operate to allow test stimulus data to be input from the test data input (TDI) pin and into the core logic unit and output to the test data output (TDO) pin. Thus, the BSCs create an architecture that allows bypassing of normal input/output signals so that test stimulus data can be transmitted through the core logic unit and output to the TDO for inspection.

TI-BSL also describes a "SAMPLE/PRELOAD" mode (see page 4), in which "the boundary scan register can be accessed via a data scan operation, to take a sample of the

functional data entering and leaving the IC." The boundary scan register is the interconnection of BSCs, such that the boundary scan register forms a horseshoe-shaped pattern around the core logic unit (see all figures on pages 3-5). Therefore, when a sample is taken of functional data entering and leaving the IC (core logic unit), this sample is actually transmitted from each BSC to another BSC along the boundary register until reaching the TDO pin. This concept is illustrated by the magnified view of a BSC shown on page 3, in which "sample data" will move up along the boundary scan register according to the position of a switch. Therefore, all samples of input data and output data are transmitted along the boundary scan register and towards a multiplexer near the TDO. Thus, TI-BSL does not describe having ***two dedicated paths*** which connect the core logic unit to a selection multiplex block for transmitting input and output data associated with the core logic unit. Even if the boundary scan register is considered a path from the core logic unit, then this is still just one path to the selection multiplex block.

Applicants note that the Office Action states the following on pages 3-4 of the Office Action:

> "TI_BSL teaches the known technique of boundary scan, where dedicated paths provided by boundary-scan cells are associated with each of the input and output pins of devices on a board (see, e.g., TI_BSL at p.3). Further, Saito alludes to the use of such boundary scan technology, for example, in paragraph [0008] (mentioning use of a "scan chain"). The input and output captured by the input and output boundary scan is further transmitted to a selection multiplex block...

Here, the Office Action states that "input and output captured by the output boundary scan is further transmitted to a selection multiplex block." However, the Office Action has not actually shown where TI-BSL describes the "at least two dedicated paths" as defined by Claim 1, and as acknowledged as missing from Saito. Applicants submit that to ***further transmit*** the input and output data along a boundary register to the selection multiplex block

is not the same as having at least two of the dedicated paths configured to transmit input data and output data from the at least one of the function blocks to the selection multiplex output block.

TI-BSL also appears to show that an instruction comes from the TDI pin (see pages 4-5) and flows through the BSCs in the boundary register to instruct the BSCs on how to operate. However, TI-BSL does not show that a processing unit transmits an instruction to the core logic unit instructing it to transmit the input and output data as debug information to a selection multiplex output block. On the contrary, TI-BSL shows that the core logic unit (as a function block) is insulated from the actual instructions associated with the boundary scan register.

During the interview, the examiner suggested that under a broad interpretation of the claims, the boundary register of TI-BSL might be considered part of the claimed "function block." However, amended Claim 1 defines that "each function block comprising one or more devices which collectively perform a specified function of the signal processor." Applicants submit that the boundary register of TI-BSL, is directed to test the operation of the core logic unit, but it is not directed to the actual function of the core logic unit itself. Therefore, Applicants submit that TI-BSL fails to disclose or suggest "each function block comprising one or more devices which collectively perform a specified function of the signal processor," as defined by amended Claim 1.

Furthermore, TI-BSL shows that the multiplexer attached to the end of the boundary register only receives a single input from the last BSC in the register. Therefore, even if the boundary register is considered part of a "function block," TI-BSL still does not show "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block ***such that the selection multiplex output block has***

at least two inputs from the at least one of the function blocks," as defined by amended Claim 1.

Therefore, Applicants submit that TI-BSL fails to disclose or suggest "at least two of the dedicated paths are provided to connect the at least one of the function blocks with the selection multiplex output block such that the selection multiplex output block has at least two inputs from the at least one of the function blocks, said at least two of the dedicated paths configured to transmit input data and output data associated with the at least one of the function blocks, as the debug information, from the at least one of the function blocks to the selection multiplex output block in response to the instruction from the processing unit," as defined by amended Claim 1.

Thus, Applicants respectfully submit that TI-BSL fails to remedy the deficiencies of Saito with regard to amended Claim 1.

Thus, Applicants respectfully submit that amended Claim 1 (and all associated dependent claims) patentably distinguishes over Saito and TI-BSL, either alone or in proper combination.

Kumiko and Edwards have been considered but fail to remedy the deficiencies of Saito and TI-BSL with regards to amended Claim 1.

Therefore, it is respectfully submitted that amended Claim 1 (and all associated dependent claims) patentably distinguish over Saito, TI-BSL, Kumiko, and Edwards, either alone or in proper combination.

Consequently, in light of the above discussion and in view of the present amendment, the outstanding grounds for rejection are believed to have been overcome. The present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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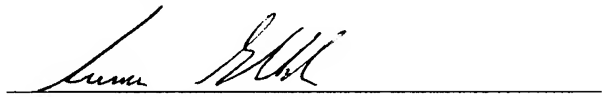

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